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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,768	04/09/2004	Chung-Ching Huang	MR3003-80	8820

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EXAMINER	
WILSON, YOLANDA L	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,768	HUANG ET AL.	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: (b)

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3,12-15,17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Yuen (USPN 5357628A). As appears in claim 1, Yuen discloses sending a system management interrupt signal to trigger a debugging tool program in column 2, lines 16-24; executing each debugging item in said debugging tool program in column 4, line 61 – column 5, line 4; and returning to current operation system after debugged in column 2, lines 31-37.

3. As per claim 2, Yuen discloses wherein said debugging tool program is provided in a system management mode of BIOS in column 2, lines 16-24.

4. As per claim 3, Yuen discloses wherein said debugging item comprises access input and output, access memory, access device configuration and trap set for specific IO address in column 4, line 61 – column 5, line 4.

5. As per claim 12, Yuen discloses a central processing unit in column 3, lines 29-30; and a chipset connected to said central processing unit in column 3, lines 30-35, including a system management interrupt pin for sending system management interrupt signal in column 5, lines 19-22, and a plurality of general purpose input/output pins for being used to trigger by users in column 4, lines 4-8.

6. As per claim 13, Yuen discloses wherein said central processing unit is connected with at lease one memory in column 4, lines 12-15.

7. As per claim 14, Yuen discloses wherein said memory comprises a system management mode section in column 4, lines 12-15.

8. As per claim 15, Yuen discloses wherein said system management mode section comprises a debugging tool program in column 5, lines 5-12.

9. As per claim 17, Yuen discloses wherein said system management interrupt signal is sent through said system management interrupt pin when said chipset triggered by users in column 4, line 61 – column 5, line 4.

10. As per claim 18, Yuen discloses wherein said system management interrupt signal is sent through the links between chipsets and central processing unit when said chipset triggered by users in column 4, line 61 – column 5, line 4.

11. As per claim 19, Yuen discloses wherein said system management interrupt signal enables said central processing unit to move into said system management mode section to execute said debugging tool program in column 4, line 61 – column 5, line 4.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 4-11,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuen in view of Dunlap (6615368B1).

14. As per claim 6, Yuen discloses a central processing unit connected to a chipset in column 3, lines 29-35, said method comprising: Sending a system management interrupt signal from said chipset to said central processing unit in column 2, lines 16-24; and Leaving the debugging operation window after end of execution in column 2, lines 31-37; Wherein finished the debugging execution, said central process unit is able to execute next queued instruction in column 2, lines 31-37.

Yuen fails to explicitly state executing to pop out a debugging operation window after said central processing unit staid in a system management mode; selecting and executing each debugging item.

Dunlap discloses this limitation in column 1, lines 39-45.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to executing to pop out a debugging operation window after said central processing unit staid in a system management mode; selecting and executing each debugging item. A person of ordinary skill in the art would have been motivated to have executing to pop out a debugging operation window after said central processing unit staid in a system management mode; selecting and executing each debugging item because the user can determine what needs to be debugged and how it is to be debugged.

15. As per claim 7, Yuen discloses wherein said debugging item comprises access input and output, access memory, access device configuration and trap set for specific IO address in column 4, line 61 – column 5, line 4.

16. As per claim 8, Yuen fails to explicitly state wherein said debugging operation window is programmable.

Dunlap discloses this limitation in column 1, lines 39-45.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have wherein said debugging operation window is programmable. A person of ordinary skill in the art would have been motivated to have wherein said debugging operation window is programmable because the user can determine what needs to be debugged and how it is to be debugged.

17. As per claim 9, Yuen discloses wherein before the step of said chipset sending said system management interrupt signal to said central processing unit in column 5, lines 19-22, said chipset is triggered by users through a predetermined general purpose input/output pin in column 4, lines 4-8.

18. As per claim 4, Yuen fails to explicitly state wherein said step of executing each debugging item in said debugging tool program could be operated in a debugging operation window.

Dunlap discloses this limitation in column 1, lines 39-45.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said step of executing each debugging item in said debugging tool program could be operated in a debugging operation window. A person of ordinary skill in the art would have been motivated to have said step of executing each debugging item in said debugging tool program could be operated in a debugging

operation window because the user can determine what needs to be debugged and how it is to be debugged.

19. As per claim 5, Yuen fails to explicitly state wherein said debugging operation window is programmable.

Dunlap discloses this limitation in column 1, lines 39-45.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have wherein said debugging operation window is programmable. A person of ordinary skill in the art would have been motivated to have wherein said debugging operation window is programmable because the user can determine what needs to be debugged and how it is to be debugged.

20. As per claim 16, Yuen fails to explicitly state wherein said debugging tool program comprises a popping out debugging operation window.

Dunlap discloses this limitation in column 1, lines 39-45.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said debugging tool program comprises a popping out debugging operation window. A person of ordinary skill in the art would have been motivated to have said debugging tool program comprises a popping out debugging operation window because the user can determine what needs to be debugged and how it is to be debugged.

21. As per claim 10, Yuen fails to explicitly state a step of after leaving said debugging operation window after end of execution, said debugging operation window would be popped out next time when said chipset triggered by users again.

Dunlap discloses this limitation in column 1, lines 39-45.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have step of after leaving said debugging operation window after end of execution, said debugging operation window would be popped out next time when said chipset triggered by users again. A person of ordinary skill in the art would have been motivated to have step of after leaving said debugging operation window after end of execution, said debugging operation window would be popped out next time when said chipset triggered by users again because the user can determine what needs to be debugged and how it is to be debugged.

22. As per claim 11, Yuen fails to explicity state a step of after leaving said debugging operation window after end of execution, said debugging operation window would be popped out from a predetermined trap address.

Dunlap discloses this limitation in column 1, lines 39-45.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have step of after leaving said debugging operation window after end of execution, said debugging operation window would be popped out from a predetermined trap address. A person of ordinary skill in the art would have been motivated to have step of after leaving said debugging operation window after end of execution, said debugging operation window would be popped out from a predetermined trap address because the user can determine what needs to be debugged and how it is to be debugged.

23. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yuen in view of Klein (20010016892A1).

24. As per claim 20, Yuen discloses wherein said chipset is presented as a south-bridge chipset.

Klein discloses this limitation in paragraph 0004.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said chipset is presented as a south-bridge chipset. A person of ordinary skill in the art would have been motivated to have said chipset is presented as a south-bridge chipset because the south bridge handles submitting smi requests.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Yolanda L Wilson
Examiner
Art Unit 2113